outer peripheral underfill resin surface, the protective resin having a surface formed so as to be flush with the inactive surface of the semiconductor chip.

19. (Amended) A semiconductor device, comprising:

a board;

a semiconductor chip joined to the board in a state where its active surface is opposite to the board and its inactive surface which is a surface on the opposite side of the active surface is exposed;

an external connecting terminal joined to a surface of the board that is facing away from the semiconductor chip, the external connecting terminal being electrically connected to the active surface of the semiconductor chip and projecting therefrom;

an underfill resin surrounding the external connecting terminal to form an outer peripheral underfill resin surface and covering at least a portion of the active surface; and

a protective resin covering a sidewall of the semiconductor chip and the outer peripheral underfill resin surface, the protective resin having a surface formed so as to be flush with the inactive surface of the semiconductor chip.

REMARKS

Claims 1, 2, 4-9 and 18-20 are pending in the application. By this Amendment, claim 3 is canceled without prejudice or disclaimer and claims 1, 2, 7, 18 and 19 are amended.

Claims 1-9 and 18-20 are rejected under 35 U.S.C. 102(a) as anticipated by Lum (U.S. Patent No. 5,959,462). The rejection is respectfully traversed.

Lum teaches a test structure for enabling burn-in testing on an entire semiconductor wafer. As shown in the Figs. 4-7, Lum teaches a semiconductor device 10 that includes a semiconductor chip 28, a protective resin 36 and an external connecting terminal.

Claim 1 is directed to a semiconductor device that includes a semiconductor chip

having an active surface and an inactive surface which is a surface on an opposite side of the active surface; protective resin covering a sidewall of the semiconductor chip and having a surface formed so as to be flush with an inactive surface of the semiconductor chip; a board on which the semiconductor chip is mounted; and an external connecting terminal joined to a surface of the board that is facing away from the semiconductor chip, the external connecting terminal being electrically connected to the active surface of the semiconductor chip.

Claim 7 is directed to a semiconductor device that includes a board; a semiconductor chip having an active surface and an inactive surface which is a surface on the opposite side of the active surface with the semiconductor chip being joined to the board in a state where the active surface thereof is facing to the board and the inactive surface thereof is exposed; and an external connecting terminal joined to a surface of the board that is facing away from the semiconductor chip, the external connecting terminal being electrically connected to the active surface of the semiconductor chip.

It is respectively submitted that claims 1 and 7 recite an external connecting terminal provided on a board on a side that is facing away from a semiconductor chip. The external connecting terminal corresponds to a solder ball 7. The solder ball 7 is electrically connected to the active surface of the semiconductor chip C via a bump 2 as the shown in Figure 2 of the application.

It is respectfully submitted that the rejection is improper because the applied art fails to teach each element of claims 1 and 7. Specifically, the applied art fails to teach an external connecting terminal joined to a surface of a board that is facing away from the semiconductor chip. In other words, the claimed invention is distinguished from Lum by the feature that the external connecting terminal is provided on the board on the side thereof facing away from the semiconductor chip. Thus, it is respectfully submitted that claims 1 and 7 are allowable over the applied art.

It is respectfully submitted that the Office Action is silent regarding any specific reasons for rejecting claims 18-20.

Claim 18 is directed to a semiconductor device that includes a semiconductor

chip having an active surface and an inactive surface disposed opposite the active surface; a board on which the semiconductor chip is mounted; an external connecting terminal joined to a surface of the board that is facing away from the semiconductor chip, the external connecting terminal being electrically connected to the active surface of the semiconductor chip and projecting therefrom; an underfill resin surrounding the external connecting terminal to form an outer peripheral underfill resin surface and covering at least a portion of the active surface; and a protective a resin covering a sidewall of the semiconductor chip and the outer peripheral underfill resin surface with the protective resin having a surface formed so as to be flush with the inactive surface of the semiconductor chip.

Claim 19 is directed to a semiconductor device that includes a board; a semiconductor chip joined to the board in a state where its active surface is opposite to the board and its inactive surface which is a surface on the opposite side of the active surface is exposed; an external connecting terminal joined to a surface of the board that is facing away from the semiconductor chip, the external connecting terminal being electrically connected to the active surface of the semiconductor chip and projecting therefrom; an underfill resin surrounding the external connecting terminal to form an outer peripheral underfill resin surface and covering at least a portion of the active surface; and a protective resin covering a sidewall of the semiconductor chip and the outer peripheral underfill resin surface with the protective resin having a surface formed so as to be flush with the inactive surface of the semiconductor chip.

Claim 20 is directed to a semiconductor device that includes a semiconductor chip having a flat inactive surface and a flat opposite active surface with a sidewall extending peripherally about the semiconductor chip and between the active surface and the inactive surface; a circuit board having a flat contacting surface disposed apart from and facially opposing the active surface of the semiconductor chip; a plurality of bumps interposed between the semiconductor chip and the circuit board for electrically connecting the active surface of the semiconductor chip and the contacting surface of the circuit board and forming a clearance among the plurality of bumps and between the active surface of the semiconductor chip and the contacting surface of the circuit

board; an underfill resin disposed between the active surface of the semiconductor chip and the contacting surface of the circuit board for filling the clearance; and a protective resin covering an outer peripheral surface of the underfill resin and the sidewall thereby surrounding the semiconductor chip and the outer peripheral surface of the underfill resin with the protective resin being in contact with and extending from the contacting surface of the circuit board to the inactive surface of the semiconductor chip to form a protective resin surface flush with the inactive surface.

Claims 18-20 recite an underfill resin.

Furthermore, claims 18 and 19 recite an external connecting terminal joined to a surface of a board that is facing away from the semiconductor chip as recited in claims 1 and 7.

Additionally, claim 20 recites a protective resin covering an outer peripheral surface of an underfill resin and a sidewall thereby surrounding a semiconductor chip and the outer peripheral surface of the underfill resin with the protective resin being in contact with and extending from a contacting surface of a circuit board to an inactive surface of the semiconductor chip to form a protective resin surface flush with the inactive surface.

It is respectfully submitted that the rejection is improper because the applied art fails to teach each element of claims 18-20. Specifically, the applied art fails to teach an underfill resin as recited in claims 18-20 as well as an external connecting terminal joined to a surface of a board that is facing away from the semiconductor chip as recited in claims 18 and 19. Also, the applied art fails to teach a protective resin covering an outer peripheral surface of an underfill resin as recited in claim 20. As a result, it is respectfully submitted that claim 18-20 are allowable over the applied art.

Claims 2 and 4-6 depend from claim 1 and include all of the features of claim 1. Claims 8 and 9 depend from claim 7 and include all of the features of claim 7. It is respectfully submitted that the dependent claims are allowable at least for the reasons the independent claims are allowable as well as for the features they recite.

Claim 3 is canceled and therefore the rejection as applied to claim 3 is now moot.

Withdrawal of the rejection is respectfully requested.

In view of the foregoing, reconsideration of the application and allowance of the pending claims are respectfully requested. Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

Should additional fees be necessary in connection with the filing of this paper or if a Petition for Extension of Time is required for timely acceptance of the same, the Commissioner is hereby authorized to charge Deposit Account No. 18-0013 for any such fees and Applicant(s) hereby petition for such extension of time.

Respectfully submitted,

Date: February 20, 2003

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Enclosure(s): Appendix I (Marked-Up Version of Amended Claims)
Petition for Extension of Time (Three Months)

DC113092

APPENDIX I

MARKED-UP VERSION OF AMENDED CLAIMS

1. (Thrice Amended) A semiconductor device, comprising:

a semiconductor chip having an active surface and an inactive surface which is a surface on an opposite side of the active surface;

protective resin covering a sidewall of the semiconductor chip and having a surface formed so as to be flush with an inactive surface of the semiconductor chip ~~which is a surface on the opposite side of an active surface of the semiconductor chip~~;

a board on which the semiconductor chip is mounted; and

an external connecting terminal joined to a surface of the board that is facing away from the semiconductor chip, the external connecting terminal being electrically connected to the active surface of the semiconductor chip ~~and projecting therefrom; and~~

~~a board, wherein the external connecting terminal is joined to a surface of the board and projects therefrom on a side opposite the semiconductor chip with respect to the board~~.

2. (Twice Amended) The semiconductor device according to claim 1, ~~wherein the external connection terminal has an exposed portion exposed to the outside of the protective resin~~ further comprising an interconnection terminal electrically connected to the active surface of the semiconductor chip and having an exposed portion exposed to the outside of the protective resin, the interconnection terminal being joined to the active surface of the semiconductor chip and to a surface of the board that is facing to the semiconductor chip, the external terminal being electrically connected to the active surface of the semiconductor chip via the interconnection terminal.

7. (Thrice Amended) A semiconductor device, comprising:

a board;

a semiconductor chip having an active surface and an inactive surface

which is a surface on the opposite side of the active surface, the semiconductor chip being joined to the board in ~~the~~ a state where ~~its~~ the active surface thereof is ~~opposite~~ facing to the board and ~~its~~ the inactive surface thereof ~~which is a surface on the opposite side of the active surface~~ is exposed; and

an external connecting terminal ~~electrically connected to the active surface of the semiconductor chip and projecting therefrom, wherein the external connecting terminal is~~ joined to a surface of the board that is facing away from the semiconductor chip, the external connecting terminal ~~projects from the surface~~ being electrically connected to the active surface of the semiconductor chip.

18. (Amended) A semiconductor device, comprising:

a semiconductor chip having an active surface and an inactive surface disposed opposite the active surface;

a board on which the semiconductor chip is mounted;

an external connecting terminal joined to a surface of the board that is facing away from the semiconductor chip, the external connecting terminal being electrically connected to the active surface of the semiconductor chip and projecting therefrom;

an underfill resin surrounding the external connecting terminal to form an outer peripheral underfill resin surface and covering at least a portion of the active surface; and

a protective a resin covering a sidewall of the semiconductor chip and the outer peripheral underfill resin surface, the protective resin having a surface formed so as to be flush with the inactive surface of the semiconductor chip.

19. (Amended) A semiconductor device, comprising:

a board;

a semiconductor chip joined to the board in ~~the~~ a state where its active surface is opposite to the board and its inactive surface which is a surface on the opposite side of the active surface is exposed;

an external connecting terminal joined to a surface of the board that is facing away from the semiconductor chip, the external connecting terminal being electrically connected to the active surface of the semiconductor chip and projecting therefrom;

an underfill resin surrounding the external connecting terminal to form an outer peripheral underfill resin surface and covering at least a portion of the active surface; and

a protective resin covering a sidewall of the semiconductor chip and the outer peripheral underfill resin surface, the protective resin having a surface formed so as to be flush with the inactive surface of the semiconductor chip.